ADwin HSM-24V

Module for LS Bus

Manual



ADwin LS Bus, Manual version 1.5, March 2010

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ADwin LS Bus, Manual version 1.5, March 2010

ADwin

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Typographical Conventions

"Warning" stands for information, which indicate damages of hardware or software, test setup or injury to persons caused by incorrect handling.



You find a "note" next to

- information, which absolutely have to be considered in order to guarantee an error free operation.
- advice for efficient operation.

"Information" refers to further information in this documentation or to other sources such as manuals, data sheets, literature, etc.

<C:\ADwin\ ...>

File names and paths are placed in <angle brackets> and characterized in the font Courier New.

Program text

Var_1

Program instructions and user inputs are characterized by the font $\ensuremath{\texttt{Courier}}$ New.

ADbasic source code elements such as instructions, variables, comments and other text are characterized by the font Courier New and are printed in color (see also the editor of the *ADbasic* development environment).

Bits in data (here: 16 bit) are referred to as follows:

Bit No.	15	14	13		01	00
Bit value	2 ¹⁵	2 ¹⁴	2 ¹³		2 ¹ =2	2 ⁰ =1
Synonym	MSB	-	-	-	-	LSB



ADwin

1 Information about this Manual

This manual describes the LS bus and the modules being operated on the LS bus. Additional information are available in

- the description of the LS bus interface in the hardware manual for *ADwin-light-16*, *ADwin-Gold* or *ADwin-Pro*.
- the manual *ADbasic*, which describes the basic instructions for the compiler of same denominator as well explains the function principle of *ADwin* systems.

The online help has the same content as the manual and additionally contains the hardware related instructions, LS bus too.

Please note:

For *ADwin* systems to function correctly, adhere strictly to the information provided in this documentation and in other mentioned manuals.

Programming, start-up and operation, as well as the modification of program parameters must be performed only by appropriately qualified personnel.

Qualified personnel are persons who, due to their education, experience and training as well as their knowledge of applicable technical standards, guidelines, accident prevention regulations and operating conditions, have been authorized by a quality assurance representative at the site to perform the necessary acivities, while recognizing and avoiding any possible dangers.

(Definition of qualified personnel as per VDE 105 and ICE 364).

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Hotline address: see inner side of cover page.

Qualified personnel

Availability of the documents



Legal information

Subject to change.

2 The LS bus

The LS bus is a bi-directional serial bus with 5MHz clock rate. The bus connects an *ADwin* system via its LS bus interface with up to 15 LS bus modules.

Figure 1 shows the standard connections of an LS bus module: Bus input and output with LED, protection earth PE, DIP switch for bus termination and bus address.



Fig. 1 - Standard connectors

The bus is set up as line connection, i.e. the interface and the LS bus modules are connected to each other via two-way links. Each module has a female DSub connector (9-pole) as bus input and a male DSub connector (9-pole) as bus output. The maximum bus length is 5 m.

The LED besides bus Bus input/output indicates data traffic on the LS bus:

- Green LED: The module receives or sends data.
- Red LED: Data for other modules is sent on the bus.
- LED off: No data traffic.

Bus Termination

Bus address

The bus termination on the last module of the LS bus must be activated with the DIP switches Term., deactivated on all other modules. To activate the bus termination both DIP switches are set down.

Each module on the LS bus is addresses via its bus address; therefore the address must be unique for each module.

The bus address is set manually with the DIP switch block on the PCB besides the bus connectors (see fig. 2). Using the 4 DIP switches Device Address the address may be set to 1...15. The setting is: 1 = DIP switch down, 0 = DIP switch up.

Address 0 disables the module. Even if a module is disabled, the folloowing modules on the LS bus receive all bus data.



Module address	Setting of DIP switches				
	1	2	3	4	
0	0	0	0	0	Module disabled
1	1	0	0	0	
2	0	1	0	0	
3	1	1	0	0	
4	0	0	1	0	
5	1	0	1	0	
15	1	1	1	1	

Fig. 2 – Module addressing with DIP switches

The GND level of the module is connected to the top hat rail, which serves as protection earth (PE). Protection earth is connected to the screw PE on the module's top.

Starten Sie *ADbasic* und booten das *ADwin*-System durch Anklicken des Boot-Schaltfläche **B**.

Protection Earth

Booten

💪 ADbasic5 - [ADbasic1]											
File	Edit	View	Build	Optic	ns	Deb	ug	Tools	W	indow	Help
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3 HSM-24V

The module HSM-24V provides 32 digital channels which process 24V signals and is operated on the LS bus.

3.1 Hardware

The 32 channels can be set to inputs or outputs in groups of 8. After power-up all channels are set as inputs.

The module requires an external supply voltage of 19V...29V. The supply connector plug is placed bottom right (see fig. 3) on the module and has each 2 pins for V_{cc} and GND. The supply voltage is led to a fuse (5A, delay-action). Both ground pins are connected to protection earth PE. The supply connection is reverse polarity safe.

The channels are designed to process 24V signals typically and are short-circuit-proof. A signal above 82% of supply voltage is processed as High level, a signal below 66% as Low level. For each channel there is a LED indicating the status: LED on relates to High level.

The channels have a permissible operation current of 0mA...150mA. If the current exceeds 500mA at a channel, the channel is automatically switched off. An over-current in the range of 150mA...500mA may activate the super-heating protection of the driver, i.e. the driver is switched off, including the corresponding 16 channels.

Each 4 channels have a common GND. The input / output wires are connected to plug-in blocks of binding posts.

The inputs have a filter causing about 12µs signal delay.

The module is easily snapped onto the DIN top hat rail. The module may be processed inside a control cabinet only (industrial use).



Fig. 3 - Board HSM-24V





The module is designed for operation in dry rooms with a room temperature of $+5^{\circ}C$... $+50^{\circ}C$ and a relative humidity of 0 ... 80% (no condensation).

3.2 RoHS Declaration of Conformity

The directive 2002/95/EG of the European Union on the restriction of the use of certain hazardous substances in electrical und electronic equipment (RoHS directive) has become operative as from 1^{st} July, 2006.

The following substances are involved:

- Lead (Pb)
- Cadmium (Cd)
- Hexavalent chromium (Cr VI)
- Polybrominated biphenyls (PBB)
- Polybrominated diphenyl ethers (PBDE)

The instructions have the following fuction:

- Mercury (Hg)

The module HSM-24V complies with the requirements of the RoHS directive.

3.3 Software

The functions of the module HSM-24V are easily programmed with *ADbasic* instructions. Please note, that instructions for the *ADwin* systems are different.

An *ADwin* process which accesses the module HSM-24V should in any case run with low priority.

If otherweise the (relatively slow) access to the module runs with high priority, all other processes have to wait and their real-time qualities may be lost. Furthermore the data connection between PC and *ADwin* system may be cut.

Instruction Function LS_DIO_INIT Initialize modul HSM-24V. LS_DIGPROG Set channels as inputs or outputs. Set level of digital outputs and return current LS_DIG_IO status. This instruction is valid for a single module only. No error handling. Set level of digital outputs. LS_DIGOUT_LONG Read current levels of digital inputs. LS_DIGIN_LONG LS_GET_OUTPUT_STATUS Read over-current status of digital outputs. Disable watchdog counter or enable and set LS_WATCHDOG_INIT watchdog time. Reset watchdog counters of all modules on LS LS_WATCHDOG_RESET bus to start values.

Fig. 5 – Instructions for HSM-24V, overview





Each set of instructions is contained in an include file; include the file appropriate to the *ADwin* system at the top of the program. The following list shows the required program lines for the *ADwin* systems and the page number where the description starts in this manual.

ADwin-light-16:	#INCLUDE	ADWL16.INC	page 7
ADwin-Gold II:	#INCLUDE	ADwinGoldII.INC	page 21
ADwin-Pro:	#INCLUDE	ADwinPRO_ALL.INC	page 37

With *ADwin-Gold II* all instructions may be used as well in *TiCoBasic* to access the HSM module. But, you have to use the include file GoldIITiCo.inc instead.



3.3.1 LS-Bus + ADwin-light-16

This section describes instructions which apply to LS bus modules connected to *ADwin-light-16*.



LS_DIO_Init	ADWIII							
LS_DIO_Init	LS_DIO_INIT initializes the specified module of type HSM-24V on the LS bus and returns the error status.							
	Syntax							
	#INCLUDE ADWL16.INC							
	ret_val = LS_DIO_INIT (ls-module)							
	Parameters							
	ls-module Specified module address on the LS bus (115).							
	ret_valBit pattern representing the error status.LONGBit = 0: No error.Bit = 1: Error occurred.							
	Bit no. 318 7 6 54 3 2 1 0							
	Status – Temp2 Temp1 – WD Time Ovr Par							
	 - :don't care (mask with 0CFh). Par:Parity error during data transfer on the LS bus. Ovr:Overrun error during data transfer on the LS bus. Time:Timeout error during data transfer on the LS bus. WD:Watchdog was released. The channel drivers are deactivated. Temp1:Superheating on driver for channels 116. Driver is deactivated. Temp2:Superheating on driver for channels 1732. Driver is deactivated. 							
	Notes							
	The instruction only be used in section INIT :, since it takes long pro- cessing time.							
	 The initialization does the following settings: All DIO channels are set as inputs. Other settings see LS_DIGPROG. The over-current status (> ca. 500mA) is reset. The error status for superheating is reset. The error status for timeout on the LS bus is reset. 							
	The error "superheating" of a driver may only occur, if over-currrent in the range of 150500mA is present on several channels at the same time. Irrespective of this, an over-current of mor than 500mA automatically switches off the concerned channel.							
	The channels of the module HSM-24V may only be operated in the range of 0150mA. This ensures the module HSM-24V is working per- manently without interruption even if all channels are used in parallel.							
	Valid for							
	HSM-24V + L16							
	See also							
	LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Digin_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset							

ADwin

Example

REM Example prozess for one module HSM-24V and ADwin-L16 **#INCLUDE** ADWL16.Inc

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1)
Par_2 = LS_DIGPROG(1, 0Fh) 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1, 1, 1100) 'watchdog time 1.1 sec
```

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels and read back real state
Par_12 = LS_DIG_IO(Par_11)



LONG

LS_DigProg

LS_DIGPROG sets the digital channels 1...32 of the specified module of type HSM-24V on the LS bus as inputs or outputs in groups of 8.

Syntax

#INCLUDE ADWL16.INC

ret_val = LS_DIGPROG(ls-module, pattern)

Parameters

ls-module	Specified module address on the LS bus (115).	LONG
pattern	Bit pattern, setting the channels as inputs or out-	LONG
	puts:	

P							
Bit =	0:	Set	char	nels	as	inpu	uts.

Bit = 1: Set channels as outputs.

Bit No.	314	3	2	1	0
Channel no.	-	32:25	24:17	16:9	8:1

ret_val Bit pattern representing the error status. Bit = 0: No error. Bit = 1: Error occurred.

Bit no.	318	7	6	54	3	2	1	0
Status	_	Temp2	Temp1	-	WD	Time	Ovr	Par

- :don't care (mask with OCFh).

Par:Parity error during data transfer on the LS bus.

Ovr:Overrun error during data transfer on the LS bus.

Time:Timeout error during data transfer on the LS bus.

WD:Watchdog was released. The channel drivers are deactivated. Temp1:Superheating on driver for channels 1...16. Driver is deactivated.

Temp2:Superheating on driver for channels 17....32. Driver is deactivated.

Notes

The instruction only be used in section **INIT**:, since it takes long processing time.

After initialization with **LS_DIO_INIT** all channels are set as inputs.

The channels may be set as inputs or outputs in groups of 8 only (4 relevant bits only, other bits are ignored).

Valid for

HSM-24V + L16

See also

LS_DIO_Init, LS_Dig_IO, LS_Digout_Long, LS_Digin_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset

ADwin

Example

REM Example prozess for one module HSM-24V and ADwin-L16 **#INCLUDE** ADWL16.Inc

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1)
Par_2 = LS_DIGPROG(1, 0Fh) 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1, 1, 1100) 'watchdog time 1.1 sec
```

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels and read back real state
Par_12 = LS_DIG_IO(Par_11)



LJ_	Dig_	U

LS_DIG_IO sets all digital outputs of the specified module HSM-24V on the LS bus to the level High oder Low and returns the status of all channels as bit pattern.

Syntax

#INCLUDE ADWL16.INC

ret_val = LS_DIG_IO(pattern)

Parameters

lametere	
pattern	Bit pattern, setting the digital outputs (see table). LONG Bit = 0: Set outputs to level Low. Bit = 1: Set outputs to level High.
ret_val	Bit pattern representing the real state of all digital LONG channels (see table). Bit = 0: Channel has level Low. Bit = 1: Channel has level High.

Bit No.	31	30	29	 2	1	0
Channel no.	32	31	30	 3	2	1

Notes

LS_DIG_IO only runs correctly, if the following conditions are given:

- There is only one module on the LS bus.
- The module is of type HSM-24V.
- The module's address is set to 1.

The channels are set as inputs or outputs using LS_DIGPROG.

The pattern is applied to those channels only, which are set as outputs. Bits for input channels are ignored.

The return value contains the real state of both inputs and outputs. The inputs have a filter causing about 12µs signal delay.

LS_DIG_IO resets the watchdog counter of the module to the start value. The counter remains enabled. The start value is set using LS_WATCHDOG_INIT.



Reset the active watchdog timer at least once to the start value within the counting interval, in order to keep the module working.

Valid for

HSM-24V + L16

See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Digin_ Long, LS_Get_Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset

ADwin

Example

REM Example prozess for one module HSM-24V and ADwin-L16 **#INCLUDE** ADWL16.Inc

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1)
Par_2 = LS_DIGPROG(1, 0Fh) 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1, 1, 1100) 'watchdog time 1.1 sec
```

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels and read back real state
Par_12 = LS_DIG_IO(Par_11)



LS_Digout_Long

LS_DIGOUT_LONG sets or clears all digital outputs of the specified module HSM-24V on the LS bus according to the transferred 32 bit value.

Syntax

#INCLUDE ADWL16.Inc

LS_DIGOUT_LONG(ls-module,pattern)

Parameters

ls-module	Specified module address on the LS bus (115).	LONG
pattern	Bit pattern, setting the digital outputs (see table).	LONG
1	Bit = 0: Set outputs to level Low.	

Bit = 1: Set outputs to level High.

Bit No.	31	30	 2	1	0
Channel no.	32	31	 3	2	1

Notes

The channels are set as inputs or outputs using LS_DIGPROG.

The pattern is applied to those channels only, which are set as outputs. Bits for input channels are ignored.

Valid for

HSM-24V + L16

See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digin_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset

Example

```
REM Example process for ADwin-L16 and 2 modules HSM-24V
REM Set process to low priority!
#INCLUDE ADWL16.Inc
```

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1) 'LS module no. 1
Par_2 = LS_DIGPROG(1, 01111b) 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1, 1, 1100) 'watchdog time 1.1 sec
```

```
Par_11 = LS_DIO_INIT(3) 'LS module no. 3
Par_12 = LS_DIGPROG(3, 0h) 'channels 1...32 as input
Par_13 = LS_WATCHDOG_INIT(3, 1, 1100) 'watchdog time 1.1 sec
```

EVENT:

```
REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels of module 1
LS_DIGOUT_LONG(1,Par_11)
REM read channels of module 3
Par_15 = LS_DIGIN_LONG(3)
REM reset watchdog
LS WATCHDOG RESET()
```



LS_Digin_Long

LS_DIGIN_LONG returns the status of all channels of the specified module HSM-24V on the LS bus as bit pattern.

Syntax

#INCLUDE ADWL16.Inc

ret_val = LS_DIGIN_LONG(ls-module)

Parameter

ls-module Specified module address on the LS bus (1...15). LONG

```
r
```

			-
0	-	770	
		va	
~	~_	• •••	_

Bit pattern representing the real state of all digital LONG

channels (see table). Bit = 0: Channel has level Low.

Bit = 1: Channel has level High.

Bit No.	31	30	 2	1	0
Channel no.	32	31	 3	2	1

Notes

We recommend to set the used channels as inputs with LS_DIGPROG before use.

The return value contains the real state of both inputs and outputs. The inputs have a filter causing about 12µs signal delay.

Valid for

HSM-24V + L16

See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset

Example

```
REM Example process for ADwin-L16 and 2 modules HSM-24V
REM Set process to low priority!
#INCLUDE ADWL16.Inc
```

INIT:

```
'10Hz HP
\mathbf{PROCESSDELAY} = 400000
                        'LS module no. 1
Par_1 = LS_DIO_INIT(1)
Par_2 = LS_DIGPROG(1, 01111b) 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1, 1, 1100) 'watchdog time 1.1 sec
```

```
Par_11 = LS_DIO_INIT(3) 'LS module no. 3
Par_12 = LS_DIGPROG(3, 0h) 'channels 1...32 as input
Par_13 = LS_WATCHDOG_INIT(3, 1, 1100) 'watchdog time 1.1 sec
```

EVENT:

REM set one channel to high, rotating from 1 to 32 **INC** Par_10 **IF** (Par_10 >= 32) **THEN** Par_10 = 0 Par_11 = SHIFT_LEFT(1,Par_10) REM set channels of module 1 LS_DIGOUT_LONG(1,Par_11) REM read channels of module 3 Par_15 = LS_DIGIN_LONG(3) REM reset watchdog LS_WATCHDOG_RESET()

HSM-24V + L16 LS_Get_Output_Status



LS_Get_Output_ Status

LS_GET_OUTPUT_STATUS returns the over-current status of outputs of the specified module HSM-24V on the LS bus as bit pattern.

Syntax

#INCLUDE ADWL16.Inc

ret_val = LS_GET_OUTPUT_STATUS(ls-module)

Parameters

ls-module	Specified module address on the LS bus (115).	LONG

 ret_val
 Bit pattern. Each bit (31...0) represents the over LONG

 current status of a digital output (see table).
 Bit = 0: Standard status.
 Bit = 1: Over-current occurred, output disabled.

Bit no.	31	30	 2	1	0
Channel no.	32	31	 3	2	1

Notes

A "superheating" error of a driver may only occur, if over-currrent in the range of 150...500mA is present on several channels at the same time. Irrespective of this, an over-current of more than 500mA automatically switches off the concerned channel.

After a "superheating" errorthe module is reset with **LS_DIO_INIT**.



The channels of the module HSM-24V may only be operated in the range of 0...150mA. This ensures the module HSM-24V is working permanently without interruption even if all channels are used in parallel.

Valid for

HSM-24V + L16

See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Digin_ Long, LS_Watchdog_Init, LS_Watchdog_Reset



REM Example process for ADwin-L16 and 2 modules HSM-24V REM Set process to low priority! **#INCLUDE** ADWL16.Inc

INIT:

PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1) 'LS module no. 1
Par_2 = LS_DIGPROG(1, 01111b) 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1, 1, 1100) 'watchdog time 1.1 sec

Par_11 = LS_DIO_INIT(3) 'LS module no. 3
Par_12 = LS_DIGPROG(3, 0h) 'channels 1...32 as input
Par_13 = LS_WATCHDOG_INIT(3, 1, 1100) 'watchdog time 1.1 sec

EVENT:

REM check for over-current
Par_5 = LS_GET_OUTPUT_STATUS(1) + LS_GET_OUTPUT_STATUS(3)
IF (Par_5 > 0) THEN END 'over-current: exit program

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels of module 1
LS_DIGOUT_LONG(1,Par_11)
REM read channels of module 3
Par_15 = LS_DIGIN_LONG(3)
REM reset watchdog
LS_WATCHDOG_RESET()



LS_Watchdog_Init	LS_WATCHD module on t started.	OG_II he LS	NIT enabl bus. If en	es or dis abled, th	ables the	e watch ter is se	dog cou et to the	nter of a start va	a specified lue and is
	Syntax								
	#INCLUDE ADWL16.INC								
	<pre>ret_val = LS_WATCHDOG_INIT(ls-module,enable,time)</pre>								
	Parameters								
	ls-module Specified module address on the LS bus (115).						LONG		
	enable		Set status 0 : Disabl 1 : Enabl	of watcl le watch e watcho	hdog co dog cou log cour	unter: nter. nter.			LONG
	time		Release ti seconds.	ime (0	107374) of the	counter	in milli-	LONG
	ret_va	1	Bit patterr Bit = 0: No Bit = 1: Er	n represe o error. rror occu	enting th rred.	e error	status.		LONG
	Bit no.	31	8 7	6	54	3	2	1	0
	Status	_	Temp2	Temp1	_	WD	Time	Ovr	Par
	- :don't ca Par:Parity Ovr:Overru Time:Time WD:Watch Temp1:Su Temp2:Su	re (ma error d un erro out err dog wa perhea perhea	sk with 0CE luring data or during da or during da as released ating on driv	Fh). transfer o ta transfe ata transf I. The cha rer for cha rer for cha	n the LS r on the l er on the annel driv annels 1. annels 17	bus. _S bus. LS bus. vers are 16. Dri '32. D	deactivat ver is dea river is de	ed. activated eactivate	l. d.
	Notes								
	The instr cessing t	uction ime.	only be u	sed in s	ection I	NIT:, 9	since it t	akes lor	ng pro-
	As long a value cor 0 (zero).	as the ntinuo If so,	watchdog usly. After the modu	counter the set re le assun	is enab elease ti nes a m	led, it d ime the alfuncti	ecremer counter on and s	nts the c value re stops; th	counter eaches nus, all

output signals are reset. After power-up of the module the counter is set to the start value 10ms and the watchdog counter is enabled.

Reset the active watchdog timer at least once to the start value within the counting interval, in order to keep the module working. To reset the module use any module specific instruction or LS_WATCHDOG_RESET.



The watchdog function is used as to monitor the connection between *ADwin* system and LS bus module.

Valid for

HSM-24V + L16

See also

LS_DIO_Init, LS_DigProg, LS_Watchdog_Reset, LS_Dig_IO, LS_ Digout_Long, LS_Digin_Long, LS_Get_Output_Status, LS_Watchdog_ Reset



REM Example prozess for one module HSM-24V and ADwin-L16 **#INCLUDE** ADWL16.Inc

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1)
Par_2 = LS_DIGPROG(1, 0Fh) 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1, 1, 1100) 'watchdog time 1.1 sec
```

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels and read back real state
Par_12 = LS_DIG_IO(Par_11)

HSM-24V + L16 LS_Watchdog_Reset

LS_Watchdog_ Reset

LS_WATCHDOG_RESET resets the watchdog counters of all modules on the LS bus to the appropriate start value. The counters remain enabled.

ADwin

Syntax

#INCLUDE ADWL16.Inc

LS_WATCHDOG_RESET()

Parameters

- / -

Notes

As long as a watchdog counter is enabled, it decrements the counter value continuously. After the set release time the counter value reaches 0 (zero). If so, the module assumes a malfunction and stops; thus, all output signals are reset.

Reset the active watchdog timer at least once to the start value within the counting interval, in order to keep the module working. To reset the module you may also use any module specific instruction.



The watchdog function is used as to monitor the connection between *ADwin* system and LS bus module.

Valid for

HSM-24V + L16

See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Digin_ Long, LS_Get_Output_Status, LS_Watchdog_Init

Example

REM Example process for ADwin-L16 and 2 modules HSM-24V REM Set process to low priority! **#INCLUDE** ADWL16.Inc

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1) 'LS module no. 1
Par_2 = LS_DIGPROG(1, 01111b) 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1, 1, 1100) 'watchdog time 1.1 sec
```

```
Par_11 = LS_DIO_INIT(3) 'LS module no. 3
Par_12 = LS_DIGPROG(3, 0h) 'channels 1...32 as input
Par_13 = LS_WATCHDOG_INIT(3, 1, 1100) 'watchdog time 1.1 sec
```

EVENT:

```
REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels of module 1
LS_DIGOUT_LONG(1,Par_11)
REM read channels of module 3
Par_15 = LS_DIGIN_LONG(3)
REM reset watchdog
LS_WATCHDOG_RESET()
```



3.3.2 LS-Bus + ADwin-Gold II

This section describes instructions which apply to LS bus modules connected to *ADwin-Gold II*.

HSM-24V + Gold II LS_DIO_Init

LS_DIO_Init

TiCo

T11

LS_DIO_INIT initializes the specified module of type HSM-24V on the LS bus and returns the error status.

ADwin

Syntax

#INCLUDE ADwinGoldII.inc / GoldIITiCo.inc

ret_val = LS_DIO_INIT(channel,ls-module)

Parameters

channel	Number (1, 2) of the LS-Bus interface.								
ls-module	Specified	LONG							
ret_val	Bit pattern representing the error status. Bit = 0: No error. Bit = 1: Error occurred.								
Bit no. 31	.8 7	6	54	3	2	1	0		
Status –	Temp2	Temp1	-	WD	Time	Ovr	Par		

- :don't care (mask with OCFh).

Par:Parity error during data transfer on the LS bus.

Ovr:Overrun error during data transfer on the LS bus.

Time:Timeout error during data transfer on the LS bus.

WD:Watchdog was released. The channel drivers are deactivated.

Temp1:Superheating on driver for channels 1...16. Driver is deactivated.

Temp2:Superheating on driver for channels 17...32. Driver is deactivated.

Notes

The instruction only be used in section **INIT**:, since it takes long processing time.

The initialization does the following settings:

- All DIO channels are set as inputs. Other settings see LS_DIGPROG.
- The over-current status (> ca. 500mA) is reset.
- The error status for superheating is reset.
- The error status for timeout on the LS bus is reset.

The error "superheating" of a driver may only occur, if over-currrent in the range of 150...500mA is present on several channels at the same time. Irrespective of this, an over-current of mor than 500mA automatically switches off the concerned channel.

The channels of the module HSM-24V may only be operated in the range of 0...150mA. This ensures the module HSM-24V is working permanently without interruption even if all channels are used in parallel.

Valid for

HSM-24V + Gold II

See also

LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Digin_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset



REM Example process for one module HSM-24V and ADwin-Gold II Rem Please select the appropriate include for ADbasic / TiCoBasic **#INCLUDE** ADwinGoldII.inc / GoldIITiCo.inc

INIT:

PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1,1) AND 0CFh
Par_2 = LS_DIGPROG(1,1,0Fh) AND 0CFh 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1,1,1,1100) AND 0CFh 'watchdog 1.1 s

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels and read back real state
Par_12 = LS_DIG_IO(1,Par_11)

HSM-24V + Gold II LS_DigProg

LS_DigProg

TiCo

T11

LS_DIGPROG sets the digital channels 1...32 of the specified module of type HSM-24V on the LS bus as inputs or outputs in groups of 8.

ADwin

Syntax

#INCLUDE ADwinGoldII.inc / GoldIITiCo.inc

```
ret_val = LS_DIGPROG(channel,ls-module,pattern)
```

Parameters

channel	Number (1	Number (1, 2) of the LS-Bus interface.								
ls-module	Specified r	Specified module address on the LS bus (115).								
pattern	Bit pattern puts: Bit = 0: Se Bit = 1: Se	Bit pattern, setting the channels as inputs or out- LONG puts: Bit = 0: Set channels as inputs. Bit = 1: Set channels as outputs.								
Bit N	lo.	314	3	2	1	0				
Cha	nnel no.	_	32:25	24:17	16:9	8:1				
ret_val	Bit pattern Bit = 0: No Bit = 1: Err	represe error. ror occur	nting th rred.	e error	status.		LONG			
Bit no. 31	.8 7	6	54	3	2	1	0			
Status –	Temp2	Temp1	-	WD	Time	Ovr	Par			

- :don't care (mask with OCFh).

Par:Parity error during data transfer on the LS bus.

Ovr:Overrun error during data transfer on the LS bus.

Time:Timeout error during data transfer on the LS bus.

WD:Watchdog was released. The channel drivers are deactivated.

Temp1:Superheating on driver for channels 1...16. Driver is deactivated.

Temp2:Superheating on driver for channels 17...32. Driver is deactivated.

Notes

The instruction only be used in section **INIT**:, since it takes long processing time.

After initialization with LS_DIO_INIT all channels are set as inputs.

The channels may be set as inputs or outputs in groups of 8 only (4 relevant bits only, other bits are ignored).

Valid for

HSM-24V + Gold II

See also

LS_DIO_Init, LS_Dig_IO, LS_Digout_Long, LS_Digin_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset



REM Example process for one module HSM-24V and ADwin-Gold II Rem Please select the appropriate include for ADbasic / TiCoBasic **#INCLUDE** ADwinGoldII.inc / GoldIITiCo.inc

INIT:

PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1,1) AND 0CFh
Par_2 = LS_DIGPROG(1,1,0Fh) AND 0CFh 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1,1,1,1100) AND 0CFh 'watchdog 1.1 s

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels and read back real state
Par_12 = LS_DIG_IO(1,Par_11)

HSM-24V + Gold II LS_Dig_IO



LS_Dig_lO	LS_DIG_IOS bus to the lev tern.	sets all digital o el High oder Lo	utput ow an	s of th Id retu	ne spe urns t	ecifie he sta	d mo atus (dule I of all	HSM-24∖ channels	on the LS as bit pat-
	Syntax									
	#INCLUDI	E ADwinGold	II.i	nc ,	/ Go	ldII	TiCo	o.in	С	
	ret_val	= LS_DIG_I	<mark>0</mark> (ch	anne	el, j	patt	ern)		
	Parameters									
	channel	channel Number (1, 2) of the LS-Bus interface.							LONG	
	pattern	Bit patter Bit = 0: S Bit = 1: S	n, set et out et out	ting t tputs tputs	he dig to lev to lev	gital c /el Lo /el Hi	outpu w. gh.	ts (se	ee table).	LONG
	ret_val	Bit patter channels Bit = 0: C Bit = 1: C	n repi (see hann hann	resen table el has el has	iting t). s leve s leve	he re el Low el Hig	al sta v. h.	ate of	all digita	LONG
		Bit No.	31	30	29		2	1	0	
		Channel no.	32	31	30		3	2	1	
	Notes									
	LS_DIG_: • The • The • The The chann The patt puts. Bits The return inputs hav LS_DIG_: ue. The c wATCHDOO	IO only runs ca ere is only one module is of the module's add nels are set as ern is applied for input channa value containa re a filter causi IO resets the vo ounter remain G_INIT.	orrect modu ype H ress input to th nels a s the ng at vatchos en	ly, if t ule or ISM- is set is or o nose o re ign real s oout 1 dog o ableo	the fo the l 24V. to 1. butpu chanr hored state 2µs counted d. The	llowir LS bu nels c l. of bot signa er of t e sta	ng co is. only, ¹ I dela he m rt va	nditic s_DI which outs a ay. odule lue is	ons are gi CGPROG. In are set and output e to the st s set usin	iven: as out- ts. The art val- ng Ls_
(P)	Reset the the counting	active watchd ng interval, in	og tir order	ner a to ke	t leas ep th	st onc e mo	e to dule	the s worki	tart value	e within
	Valid for									
	HSM-24V	+ Gold II								
	See also									
	LS_DIO_I Output_St	nit, LS_DigPro atus, LS_Wato	g, LS hdog	5_Dig J_Init,	out_L LS_\	.ong, Watcł	LS_[ndo <u>g</u>	Digin_ _Res	_Long, LS et	S_Get_



REM Example process for one module HSM-24V and ADwin-Gold II Rem Please select the appropriate include for ADbasic / TiCoBasic **#INCLUDE** ADwinGoldII.inc / GoldIITiCo.inc

INIT:

PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1,1) AND 0CFh
Par_2 = LS_DIGPROG(1,1,0Fh) AND 0CFh 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1,1,1,1100) AND 0CFh 'watchdog 1.1 s

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels and read back real state
Par_12 = LS_DIG_IO(1,Par_11)

HSM-24V + Gold II LS_Digout_Long

TiCo

T11

LS_Digout_Long

LS_DIGOUT_LONG sets or clears all digital outputs of the specified module HSM-24V on the LS bus according to the transferred 32 bit value.

Syntax

```
#INCLUDE ADwinGoldII.inc / GoldIITiCo.inc
```

```
LS_DIGOUT_LONG(channel, ls-module, pattern)
```

Parameters

channel	Number (1, 2) of the LS-Bus interface.
ls-module pattern	Specified module address on the LS bus (115). LONG Bit pattern, setting the digital outputs (see table). LONG Bit = 0: Set outputs to level Low. Bit = 1: Set outputs to level High.
1	Pit No. 21 20 2 1 0

Bit No.	31	30	 2	1	0
Channel no.	32	31	 3	2	1

Notes

The channels are set as inputs or outputs using LS_DIGPROG.

The pattern is applied to those channels only, which are set as outputs. Bits for input channels are ignored.

Valid for

HSM-24V + Gold II

See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, , LS_Digin_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset

ADwin

Example

REM Example process for ADwin-Gold II and 2 modules HSM-24V REM Set process to low priority! Rem Please select the appropriate include for ADbasic / TiCoBasic **#INCLUDE** ADwinGoldII.inc / GoldIITiCo.inc

INIT:

PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1,1) AND 0CFh
Par_2 = LS_DIGPROG(1,1,0Fh) AND 0CFh 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1,1,1,1100) AND 0CFh 'watchdog 1.1 s

Par_11 = Ls_DIO_INIT(1,3)'LS module no. 3
Par_12 = Ls_DIGPROG(1,3,0h) 'channels 1...32 as input
Par_13 = Ls_WATCHDOG_INIT(1,3,1,1100) 'watchdog time 1.1 sec

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels of module 1
LS_DIGOUT_LONG(1,1,Par_11)
REM read channels of module 3
Par_15 = LS_DIGIN_LONG(1,3)
REM reset watchdog
LS_WATCHDOG_RESET(1)

LS_Digin_Long

TiCo

T11

LS_DIGIN_LONG returns the status of all channels of the specified module HSM-24V on the LS bus as bit pattern.

ADwin

Syntax

```
#INCLUDE ADwinGoldII.inc / GoldIITiCo.inc
```

```
ret_val = LS_DIGIN_LONG(module, channel, ls-module)
```

Parameters

channel	Number (1, 2) of the LS-Bus interface.
ls-module	Specified module address on the LS bus (115). $\hfill LONG$
ret_val	Bit pattern representing the real state of all digital LONG channels (see table). Bit = 0: Channel has level Low. Bit = 1: Channel has level High.

Bit No.	31	30	 2	1	0
Channel no.	32	31	 3	2	1

Notes

We recommend to set the used channels as inputs with **LS_DIGPROG** before use.

The return value contains the real state of both inputs and outputs. The inputs have a filter causing about $12\mu s$ signal delay.

Valid for

HSM-24V + Gold II

See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset

ADwin

Example

REM Example process for ADwin-Gold II and 2 modules HSM-24V REM Set process to low priority! Rem Please select the appropriate include for ADbasic / TiCoBasic **#INCLUDE** ADwinGoldII.inc / GoldIITiCo.inc

INIT:

PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1,1) AND 0CFh 'LS module no. 1
Par_2 = LS_DIGPROG(1,1,0Fh) AND 0CFh 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1,1,1,1100) AND 0CFh 'watchdog 1.1 s

Par_11 = LS_DIO_INIT(1,3) AND 0CFh 'LS module no. 1
Par_12 = LS_DIGPROG(1,3,0h) AND 0CFh 'channels 1...32 as input
Par_13 = LS_WATCHDOG_INIT(1,3,1,1100) AND 0CFh 'watchdog 1.1 s

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels of module 1
LS_DIGOUT_LONG(1,1,Par_11)
REM read channels of module 3
Par_15 = LS_DIGIN_LONG(1,3)
REM reset watchdog
LS_WATCHDOG_RESET(1)

HSM-24V + Gold II LS_Get_Output_Status

LS_Get_Output_ Status

LS_GET_OUTPUT_STATUS returns the over-current status of outputs of the specified module HSM-24V on the LS bus as bit pattern.

ADwin

Syntax

```
#INCLUDE ADwinGoldII.inc / GoldIITiCo.inc
```

```
ret_val = LS_GET_OUTPUT_STATUS(channel, ls-module)
```

Parameters

channel	Number (1, 2) of the LS-Bus interface.
ls-module	Specified module address on the LS bus (115). $\hfill LONG$
ret_val	Bit pattern. Each bit (310) represents the over- LONG current status of a digital output (see table). Bit = 0: Standard status. Bit = 1: Over-current occurred, output disabled.
	Bit no. 31 30 2 1 0

3

2

1

Notes

A "superheating" error of a driver may only occur, if over-currrent in the range of 150...500 mA is present on several channels at the same time. Irrespective of this, an over-current of more than 500 mA automatically switches off the concerned channel.

31

...

After a "superheating" errorthe module is reset with **LS_DIO_INIT**.

32

The channels of the module HSM-24V may only be operated in the range of 0...150mA. This ensures the module HSM-24V is working permanently without interruption even if all channels are used in parallel.

Valid for

HSM-24V + Gold II

Channel no.

See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Digin_ Long, LS_Watchdog_Init, LS_Watchdog_Reset



ADwin

Example

REM Example process for ADwin-Gold II and 2 modules HSM-24V REM Set process to low priority! Rem Please select the appropriate include for ADbasic / TiCoBasic **#INCLUDE** ADwinGoldII.inc / GoldIITiCo.inc

INIT:

PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1,1) AND 0CFh 'LS module no. 1
Par_2 = LS_DIGPROG(1,1,0Fh) AND 0CFh 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1,1,1,1100) AND 0CFh 'watchdog 1.1 s

Par_11 = LS_DIO_INIT(1,3) AND 0CFh 'LS module no. 1
Par_12 = LS_DIGPROG(1,3,0h) AND 0CFh 'channels 1...32 as input
Par_13 = LS_WATCHDOG_INIT(1,3,1,1100) AND 0CFh 'watchdog 1.1 s

EVENT:

```
REM check for over-current
Par_5 = LS_GET_OUTPUT_STATUS(1,1) + LS_GET_OUTPUT_STATUS(1,3)
IF (Par_5>0) THEN END 'over-current: exit program
REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels of module 1
LS_DIGOUT_LONG(1,1,Par_11)
REM read channels of module 3
Par_15 = LS_DIGIN_LONG(1,3)
REM reset watchdog
LS_WATCHDOG_RESET(1)
```



LS_Watchdog_Init	LS_WATCHDOG_INIT enables or disables the watchdog counter of a specified module on the LS bus. If enabled, the counter is set to the start value and is started.								
	Syntax								
	#INCLUDE ADwi	nGoldII.inc /	GoldI	ITiC	Co.inc				
	ret_val = LS_W time)	ATCHDOG_INIT ((channe	el,1:	s-modu]	le,ena	ble,		
	Parameters								
	channel Number (1, 2) of the LS-Bus interface.								
	ls-module Sp	ecified module ad	dress or	n the	LS bus (115).	LONG		
	enable Se 0: 1:	t status of watchd Disable watchdo Enable watchdog	log coun og counte g counte	ter: er. er.			LONG		
	time Re	Release time (0107374) of the counter in milli-							
LS_Watchdog_Ini	ret_val Bit Bit Bit	pattern represent = 0: No error. = 1: Error occurre	ting the e	error	status.		LONG		
	Bit no. 318	7 6 5	54	3	2	1	0		
	Status –	Temp2 Temp1	- \	WD	Time	Ovr	Par		
	Par:Parity error durin Ovr:Overrun error du Time:Timeout error du WD:Watchdog was Temp1:Superheating Temp2:Superheating	ang data transfer on t uring data transfer o during data transfer eleased. The chanr g on driver for chanr g on driver for chanr	the LS but on the LS on the LS nel drivers nels 11 nels 17	is. bus. S bus. s are o 6. Driv 32. Di	deactivate ver is dea river is de	ed. activated	l. d.		
	Notes								
	The instruction only be used in section INIT :, since it takes long pro- cessing time.								
	As long as the watchdog counter is enabled, it decrements the counter value continuously. After the set release time the counter value reaches 0 (zero). If so, the module assumes a malfunction and stops; thus, all output signals are reset.								
	After power-up of the module the counter is set to the start value 10ms and the watchdog counter is enabled.								
	Reset the active the counting inter- module use any n	vatchdog timer at val, in order to kee nodule specific ins	least or ep the m struction	nce to Iodule or La	o the sta e working 5_watCf	rt value g. To re IDOG_R	e within set the ESET.		
	The watchdog fur <i>ADwin</i> system an	nction is used as t d LS bus module.	to monit	or the	e conne	ction be	etween		
	Valid for								
	HSM-24V + Gold	II							
. .									



See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Digin_ Long, LS_Get_Output_Status, LS_Watchdog_Reset

Example

REM Example process for one module HSM-24V and ADwin-Gold II Rem Please select the appropriate include for ADbasic / TiCoBasic **#INCLUDE** ADwinGoldII.inc / GoldIITiCo.inc

INIT:

PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1,1) AND 0CFh 'LS module no. 1
Par_2 = LS_DIGPROG(1,1,0Fh) AND 0CFh 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1,1,1,1100) AND 0CFh 'watchdog 1.1 s

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels and read back real state
Par_12 = LS_DIG_IO(1,Par_11)

HSM-24V + Gold II LS_Watchdog_Reset

LS_Watchdog_ Reset



LS_WATCHDOG_RESET resets the watchdog counters of all modules on the LS bus to the appropriate start value. The counters remain enabled.

Syntax

```
#INCLUDE ADwinGoldII.inc / GoldIITiCo.inc
```

LS_WATCHDOG_RESET(channel)

Parameters

channel Number (1, 2) of the LS-Bus interface.

Notes

As long as a watchdog counter is enabled, it decrements the counter value continuously. After the set release time the counter value reaches 0 (zero). If so, the module assumes a malfunction and stops; thus, all output signals are reset.

Reset the active watchdog timer at least once to the start value within the counting interval, in order to keep the module working. To reset the module you may also use any module specific instruction.

The watchdog function is used as to monitor the connection between *ADwin* system and LS bus module.

Valid for

HSM-24V + Gold II

See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Digin_ Long, LS_Get_Output_Status, LS_Watchdog_Init

Example

REM Example process for ADwin-Gold II and 2 modules HSM-24V REM Set process to low priority! Rem Please select the appropriate include for ADbasic / TiCoBasic **#INCLUDE** ADwinGoldII.inc / GoldIITiCo.inc

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1,1) AND 0CFh 'LS module no. 1
Par_2 = LS_DIGPROG(1,1,0Fh) AND 0CFh 'channels 1...32 as output
Par_3 = LS_WATCHDOG INIT(1,1,1,1100) AND 0CFh 'watchdog 1.1 s
```

Par_11 = LS_DIO_INIT(1,3)'LS module no. 3
Par_12 = LS_DIGPROG(1,1,0h) 'channels 1...32 as input
Par_13 = LS_WATCHDOG_INIT(1,1,1,1100) 'watchdog time 1.1 sec

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels of module 1
LS_DIGOUT_LONG(1,1,Par_11)
REM read channels of module 3
Par_15 = LS_DIGIN_LONG(1,3)
REM reset watchdog
LS WATCHDOG RESET(1)

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LONG



3.3.3 LS-Bus + Pro I

This section describes instructions which apply to Pro I LS bus modules:

- LS_DIO_Init (page 38)
- LS_DigProg (page 40)
- LS_Dig_IO (page 42)
- LS_Digout_Long (page 44)
- LS_Digin_Long (page 46)
- LS_Get_Output_Status (page 48)
- LS_Watchdog_Init (page 50)
- LS_Watchdog_Reset (page 52)

LS



DIO_Init	LS_DIO_INIT ir via an interface c	iitializes the of the Pro m	e specifie nodule ar	d modul nd returr	e of typ is the e	e HSM-2 rror stat	24V on t us	he LS bus
	Syntax							
	#INCLUDE A	DwinPro_A	All.Ind	2				
	ret_val =	LS_DIO_II	NIT (moo	dule,cl	nannel	.ls-mo	odule)	
	Parameters							
	module	Specified	module a	address	(125	5).		LONG
	channel	number (1 module.	1, 2) of tl	ne LS bi	us inter	face on	the Pro	LONG
	ls-module	Specified	module a	address	on the	LS bus (115).	LONG
module. ls-module Specified module address on the LS bus (115). ret_val Bit pattern representing the error status. Bit = 0: No error. Bit = 1: Error occurred.								LONG
	Bit no. 31	.8 7	6	54	3	2	1	0
	Status –	Temp 2	Temp 1	_	WD	Time	Ovr	Par
	- :don't care (ma Par:Parity error Ovr:Overrun err	ask with OCF during data t or during dat	h). transfer o ta transfe	n the LS r on the L	bus. S bus.			

Time:Timeout error during data transfer on the LS bus. WD:Watchdog was released. The channel drivers are deactivated.

Temp1:Superheating on driver for channels 1...16. Driver is deactivated. Temp2:Superheating on driver for channels 17...32. Driver is deactivated.

Notes

The instruction only be used in section **INIT**:, since it takes long processing time.

The initialization does the following settings:

- All DIO channels are set as inputs. Other settings see LS_DIGPROG.
- The over-current status (> ca. 500mA) is reset.
- The error status for superheating is reset.
- The error status for timeout on the LS bus is reset.

The error "superheating" of a driver may only occur, if over-currrent in the range of 150...500mA is present on several channels at the same time. Irrespective of this, an over-current of mor than 500mA automatically switches off the concerned channel.



The channels of the module HSM-24V may only be operated in the range of 0...150mA.

Valid for

LS-2 Rev. A

See also

LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Digin_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset



REM Example prozess for one module HSM-24V and ADwin-Pro-LS2 **#INCLUDE** ADwinPro_All.Inc

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
Par_1 = LS_DIO_INIT(1,2,1)
Par_2 = LS_DIGPROG(1,2,1,0Fh) 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(1,2,1,1,1100) 'watchdog time 1.1 sec
```

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels and read back real state
Par_12 = LS_DIG_IO(1,2,Par_11)



LS_DigProg	LS_DIGPROG sets the digital channels 132 of the specified module of type HSM-24V on the LS bus as inputs or outputs in groups of 8 via an interface of the Pro module.									
	Syntax									
	#INCLUDE ADwinPro_All.Inc									
	<pre>ret_val = LS_DIGPROG(module,channel,ls-module,</pre>									
	G LS_DIGPROC sets the digital channels 132 of the specified module of type HSM-24V on the LS bus as inputs or outputs in groups of 8 via an interface of the Pro module. Syntax #INCLUDE ADwinPro_All.Inc ret_val = LS_DIGPROG(module, channel, ls-module, pattern) Parameters module Specified module address (1255). LONG channel number (1, 2) of the LS bus interface on the Pro LONG module Specified module address on the LS bus (115). LONG pattern Bit pattern, setting the channels as inputs or out-LONG puts: Bit = 0: Set channels as inputs. Bit = 1: Set channels as outputs. Bit = 1: Set channels as outputs. Bit = 0: No error. Bit = 1: Error occurred. <u>Bit no. 318 7 6 54 3 2 1 0</u> Status - Temp Temp - WD Time Ovr Par 2 1 - :dont care (mask with OCPh). ParParity error during data transfer on the LS bus. Vn:Overun error during data transfer on the LS bus. WD:Watchdog was released. The channel drivers are deactivated. Temp1:Superheating on driver for channels 116. Driver is deactivated. Temp2:Superheating on driver for channels 116. Driver is deactivated. The instruction only be used in section INIT :, since it takes long processing time. After initialization with LS_DIO_INIT all channels are set as inputs.									
	module Specified module address (1255).									
	channel number (1, 2) of the LS bus interface on the Pro LONG module.									
	ls-module Specified module address on the LS bus (115). LONG									
	patternBit pattern, setting the channels as inputs or out-LONGputs:Bit = 0: Set channels as inputs.Bit = 1: Set channels as outputs.									
	Bit No. 31 4 3 2 1 0									
	Channel no. – 32:25 24:17 16:9 8:1									
LS_DIgProg	ret_valBit pattern representing the error status.LONGBit = 0: No error.Bit = 1: Error occurred.									
	Bit no. 318 7 6 54 3 2 1 0									
	Status – Temp Temp – WD Time Ovr Par 2 1									
	HSM-24V on the LS bus as inputs or outputs in groups of 8 via an interface the Pro module. Syntax #INCLUDE ADwinPro_All.Inc ret_val = LS_DIGPROG(module,channel,ls-module, pattern) Parameters module Specified module address (1255). LOW channel number (1, 2) of the LS bus interface on the Pro LOW module. ls-module Specified module address on the LS bus (115). LOW pattern Bit pattern, setting the channels as inputs or out- puts: Bit = 0: Set channels as inputs. Bit = 0: Set channels as outputs. Bit = 0: Set channels as outputs. If the thermodule address on the LS bus (115). LOW puts: Bit = 0: Set channels as outputs. If the thermodule address on the LS bus (115). LOW puts: Bit = 0: Set channels as outputs. If the thermodule address on the LS bus (115). LOW puts: Bit = 0: No error. Bit = 1: Error occurred. Distatus - Temp Temp - WD Time Ovr Par 2 1 - :don't care (mask with 0CFh). Par.Parity error during data transfer on the LS bus. Ov:Overrun error during data transfer on the LS bus. WD:Watchdog was released. The channel drivers are deactivated. Teme:Timeout error during data transfer on the LS bus. WD:Watchdog was released. The channel frivers are deactivated. Temp:Superheating on driver for channels 116. Driver is deactivated. Temp:Superheating on driver for channels 117. Since it takes long pro- cessing time. After initialization with LS_DIO_INIT all channels are set as inputs. The channels may be set as inputs or outputs in groups of 8 only (4 rel- evant bits only, other bits are ignored).									
Bit = 1: Set channels as outputs. Bit No. 314 3 2 Channel no. - 32:25 24:17 ret_val Bit pattern representing the error s Bit = 0: No error. Bit = 0: No error. Bit = 1: Error occurred. Bit no. 318 7 6 54 3 Status - Temp Temp - WD 2 1 - :don't care (mask with 0CFh). Par:Parity error during data transfer on the LS bus. Ovr:Overrun error during data transfer on the LS bus. Ovr:Overrun error during data transfer on the LS bus. WD:Watchdog was released. The channel drivers are d Temp1:Superheating on driver for channels 116. Driv Temp2:Superheating on driver for channels 1732. Dri Notes The instruction only be used in section INIT:, si cessing time. After initialization with LS_DIO_INIT all channels	Notes									
	The instruction only be used in section INIT :, since it takes long pro- cessing time.									
	After initialization with Ls_DIO_INIT all channels are set as inputs.									
	The channels may be set as inputs or outputs in groups of 8 only (4 rel- evant bits only, other bits are ignored).									

Valid for

LS-2 Rev. A

See also

LS_DIO_Init, LS_Dig_IO, LS_Digout_Long, LS_Digin_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset



REM Example prozess for one module HSM-24V and ADwin-Pro-LS2 **#INCLUDE** ADwinPro_All.Inc

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
PAR_1 = LS_DIO_INIT(1,2,1)
PAR_2 = LS_DIGPROG(1,2,1,0Fh) 'channels 1...32 as output
PAR_3 = LS_WATCHDOG_INIT(1,2,1,1,1100) 'watchdog time 1.1 sec
```

EVENT:

REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
PAR_11 = SHIFT_LEFT(1,PAR_10)
REM set channels and read back real state
PAR_12 = LS_DIG_IO(1,2,PAR_11)



_S_Dig_10									
LS_Dig_IO	LS_DIG_IO sets all digital outputs of the specified module HSM-24V on the LS bus to the level High oder Low and returns the status of all channels as bit pattern.								
	Syntax								
	#INCLUDE ADwinPro_All.Inc								
	<pre>ret_val = LS_DIG_IO(module, channel, pattern)</pre>								
	Parameters								
	module Specified module address (1255).								
	channel number (1, 2) of the LS bus interface on the Pro LONG module.								
	patternBit pattern, setting the digital outputs (see table).LONGBit = 0: Set outputs to level Low.Bit = 1: Set outputs to level High.								
	ret_valBit pattern representing the real state of all digital LONG channels (see table).Bit = 0: Channel has level Low. Bit = 1: Channel has level High.								
	Bit No. 31 30 29 2 1 0								
	Channel no. 32 31 30 3 2 1								
	Notes								
(j)	 LS_DIG_IO only runs correctly, if the following conditions are given: There is only one module on the LS bus. The module is of type HSM-24V. The module's address is set to 1. 								
	The channels are set as inputs or outputs using LS_DIGPROG.								
	The pattern is applied to those channels only, which are set as outputs. Bits for input channels are ignored.								
	The return value contains the real state of both inputs and outputs. The inputs have a filter causing about $12\mu s$ signal delay.								
	LS_DIG_IO resets the watchdog counter of the module to the start va- lue. The counter remains enabled. The start value is set using LS_ WATCHDOG_INIT.								
	Reset the active watchdog timer at least once to the start value within the counting interval, in order to keep the module working.								
	Valid for								
	LS-2 Rev. A								
	See also								
	LS_DIO_Init, LS_DigProg, LS_Digout_Long, LS_Digin_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset								



REM Example prozess for one module HSM-24V and ADwin-Pro-LS2 **#INCLUDE** ADwinPro_All.Inc

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
PAR_1 = LS_DIO_INIT(1,2,1)
PAR_2 = LS_DIGPROG(1,2,1,0Fh) 'channels 1...32 as output
PAR_3 = LS_WATCHDOG_INIT(1,2,1,1,1100) 'watchdog time 1.1 sec
```

EVENT:

```
Rem check for over-current
PAR_5 = Ls_GET_OUTPUT_STATUS(3,1,2)
PAR_5 = PAR_5 + Ls_GET_OUTPUT_STATUS(3,1,4)
IF (PAR_5>0) THEN END 'over-current: Exit program
```

```
REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
Rem set channels of LS module 2
LS_DIGOUT_LONG(3,1,2,PAR_11)
Rem read channels of LS module 4
PAR_15 = LS_DIGIN_LONG(3,1,4)
Rem reset watchdog
LS_WATCHDOG_RESET(3,1)
```

LS_Digout_Long

LS_DIGOUT_LONG sets or clears all digital outputs of the specified module HSM-24V on the LS bus according to the transferred 32 bit value.

ADwin

1

Syntax

#INCLUDE ADwinPro_All.Inc

Channel no.

LS_DIGOUT_LONG(module,channel,ls-module,pattern)

Parameters

module	Specified module address (1255).
channel	number (1, 2) of the LS bus interface on the Pro LONG module.
ls-module	Specified module address on the LS bus (115). LONG
pattern	Bit pattern, setting the digital outputs (see table). LONG Bit = 0: Set outputs to level Low. Bit = 1: Set outputs to level High.
	Bit No. 31 30 2 1 0

Notes

The channels are set as inputs or outputs using LS_DIGPROG.

32

The pattern is applied to those channels only, which are set as outputs. Bits for input channels are ignored.

31

...

3

2

Valid for

LS-2 Rev. A

See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digin_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset



REM Example process for ADwin-Pro and 2 modules HSM-24V REM Set process to low priority! **#INCLUDE** ADwinPro_All.Inc

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
REM Settings for LS module 2 via Pro module 3, channel 1
Par_1 = LS_DIO_INIT(3,1,2)
Par_2 = LS_DIGPROG(3,1,2,01111b) 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(3,1,2, 1, 1100) 'watchdog time 1.1 sec
```

```
REM Settings for LS module 4 via Pro module 3, channel 1
Par_11 = LS_DIO_INIT(3,1,4)
Par_12 = LS_DIGPROG(3,1,4, 0h) 'channels 1...32 as input
Par_13 = LS_WATCHDOG_INIT(3,1,4, 1, 1100) 'watchdog time 1.1 sec
```

EVENT:

```
REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels of LS module 2
LS_DIGOUT_LONG(3,1,2,Par_11)
REM read channels of LS module 4
Par_15 = LS_DIGIN_LONG(3,1,4)
REM reset watchdog
LS_WATCHDOG_RESET(3,1)
```



See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Get_ Output_Status, LS_Watchdog_Init, LS_Watchdog_Reset

ADwin



REM Example process for ADwin-Pro and 2 modules HSM-24V REM Set process to low priority! **#INCLUDE** ADwinPro_All.Inc

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
REM Settings for LS module 2 via Pro module 3, channel 1
Par_1 = LS_DIO_INIT(3,1,2)
Par_2 = LS_DIGPROG(3,1,2,01111b) 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(3,1,2, 1, 1100) 'watchdog time 1.1 sec
```

```
REM Settings for LS module 4 via Pro module 3, channel 1
Par_11 = LS_DIO_INIT(3,1,4)
Par_12 = LS_DIGPROG(3,1,4, 0h) 'channels 1...32 as input
Par_13 = LS_WATCHDOG_INIT(3,1,4, 1, 1100) 'watchdog time 1.1 sec
```

EVENT:

```
REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels of LS module 2
LS_DIGOUT_LONG(3,1,2,Par_11)
REM read channels of LS module 4
Par_15 = LS_DIGIN_LONG(3,1,4)
REM reset watchdog
LS_WATCHDOG_RESET(3,1)
```



LS_Get_Output_ Status	LS_GET_OUTPUT_STATUS returns the over-current status of outputs of the specified module HSM-24V on the LS bus as bit pattern.									
	Syntax									
	#INCLUDE A	ADwinPro_Al	l.In	IC						
	ret_val = module)	<pre>ret_val = LS_GET_OUTPUT_STATUS(module,channel,ls- module)</pre>								S-
	Parameters module	Specified me	odule	addr	ess (′	125	55).			LONG
	channel	number (1, module.	2) of 1	the L	S bus	s inte	rface	on tl	he Pro	LONG
	ls-module	Specified me	odule	addr	ess o	n the	LS b	ous (1	l15).	LONG
	ret_val	Bit pattern. current statu Bit = 0: Stan Bit = 1: Ove	Each is of a dard r-curr	bit (3 a digi statu ent o	(10) tal ou s. ccurre) repr tput (ed, ou	resen (see t utput	ts the able) disat	e over-). bled.	LONG
		Bit no.	31	30		2	1	0	Ī	
	-	Channel no.	32	31		3	2	1	_	
	Notes									
(B)	A "superheating" error of a driver may only occur, if over-curr range of 150500mA is present on several channels at the s Irrespective of this, an over-current of more than 500mA aut switches off the concerned channel. After a "superheating" errorthe module is reset with LS_DIO The channels of the module HSM-24V may only be operation range of 0						currren ne sam automa IO_IN erated s workin	t in the e time. atically IT. in the ng per-		
	manentiy wit						5 010	uset	u in pai	rallei.
	Valid for LS-2 Rev. A									
	See also LS_DIO_Init, Long, LS_Wa	, LS_DigProg atchdog_Init, L	, LS_ .S_W	Dig_l atchd	IO, LS log_R	S_Dig leset	gout_	Long	g, LS_I	Digin_



REM Example process for ADwin-Pro and 2 modules HSM-24V REM Set process to low priority! **#INCLUDE** ADwinPro_All.Inc

INIT:

```
PROCESSDELAY = 4000000 '10Hz HP
REM Settings for LS module 2 via Pro module 3, channel 1
Par_1 = LS_DIO_INIT(3,1,2)
Par_2 = LS_DIGPROG(3,1,2,01111b) 'channels 1...32 as output
Par_3 = LS_WATCHDOG_INIT(3,1,2, 1, 1100) 'watchdog time 1.1 sec
```

```
REM Settings for LS module 4 via Pro module 3, channel 1
Par_11 = LS_DIO_INIT(3,1,4)
Par_12 = LS_DIGPROG(3,1,4, 0h) 'channels 1...32 as input
Par_13 = LS_WATCHDOG_INIT(3,1,4, 1, 1100) 'watchdog time 1.1 sec
```

EVENT:

```
REM set one channel to high, rotating from 1 to 32
INC Par_10
IF (Par_10 >= 32) THEN Par_10 = 0
Par_11 = SHIFT_LEFT(1,Par_10)
REM set channels of LS module 2
LS_DIGOUT_LONG(3,1,2,Par_11)
REM read channels of LS module 4
Par_15 = LS_DIGIN_LONG(3,1,4)
REM reset watchdog
LS_WATCHDOG_RESET(3,1)
```



LO_Wateriaog_init										
LS_Watchdog_Init	LS_WATCHDOG module on the	J_I LS	NIT enable bus via ar	es or dis interfac	ables the	e watch Pro mo	dog cou odule.	nter of a	a specified	
	Syntax									
	#INCLUDE ADwinPro_All.Inc									
	ret_val = ls-mo	= L odu	ls_watChi ile, enab	DOG_IN	IT(mod ime)	ule, c	channel	- 1		
	Parameters									
	module		Specified I	module	address	(125	5).		LONG	
	channel		number (1, 2) of the LS bus interface on the Pr module.						LONG	
	ls-modul	ale Specified module address on the LS bus (11						115).	LONG	
	enable		Set status 0 : Disabl 1 : Enable	of watch e watch e watcho	hdog co dog cou dog cour	unter: nter. nter.			LONG	
	time		Release ti seconds.	me (0	107374) of the	counter	in milli-	LONG	
	ret_val		Bit pattern representing the error status. Bit = 0:No error. Bit = 1: Error occurred.						LONG	
	Bit no. 3	1	8 7	6	54	3	2	1	0	
	Status	-	Temp 2	Temp 1	-	WD	Time	Ovr	Par	
	 - :don't care (mask with 0CFh) Par:Parity error during data transfer on the LS bus. Ovr: Overrun error during data transfer on the LS bus. Time: Timeout error during data transfer on the LS bus. WD: Watchdog was released. The channel drivers are deactivated. Temp1: Superheating on driver for channels 116. Driver is deactivated. Temp2: Superheating on driver for channels 1732. Driver is deactivated. 									
	Notes									
	The instruction only be used in section INIT :, since it takes long pro- cessing time.									
	As long as the watchdog counter is enabled, it decrements the counter value continuously. After the set release time the counter value reaches 0 (zero). If so, the module assumes a malfunction and stops; thus, all output signals are reset.									
	After power and the wat	r-up tcha	o of the moo	dule the r is enal	counter bled.	is set t	o the sta	irt value	e 10ms	
	Reset the active watchdog timer at least once to the start value within the counting interval, in order to keep the module working. To reset the									



The watchdog function is used as to monitor the connection between *ADwin* system and LS bus module.

module use any module specific instruction or LS_WATCHDOG_RESET.

Valid for

LS-2 Rev. A



See also

LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Digin_ Long, LS_Get_Output_Status, LS_Watchdog_Reset

Example

REM Example prozess for one module HSM-24V and ADwin-Pro-LS2 **#INCLUDE** ADwinPro_All.Inc

INIT:

PROCESSDELAY = 4000000 '10Hz HP
PAR_1 = Ls_DIO_INIT(1,2,1)
PAR_2 = Ls_DIGPROG(1,2,1,0Fh) 'channels 1...32 as output
PAR_3 = Ls_WATCHDOG_INIT(1,2,1,1,1100) 'watchdog time 1.1 sec

EVENT:

REM set one channel to high, rotating from 1 to 32
INC PAR_10
IF (PAR_10 >= 32) THEN PAR_10 = 0
PAR_11 = SHIFT_LEFT(1,PAR_10)
REM set channels and read back real state
PAR_12 = LS_DIG_IO(1,2,PAR_11)



LS_Watchdog_ Reset	LS_WATCHDOG_RESET resets the watchdog counters of all modules on the LS bus to the appropriate start value. The counters remain enabled.
	Syntax
	#INCLUDE ADwinPro_All.Inc
	LS_WATCHDOG_RESET (module, channel)
	Parameters
	module Specified module address (1255).
	channel number (1, 2) of the LS bus interface on the Pro LONG module.
	Notes
	As long as a watchdog counter is enabled, it decrements the counter value continuously. After the set release time the counter value reaches 0 (zero). If so, the module assumes a malfunction and stops; thus, all output signals are reset.
	Reset the active watchdog timer at least once to the start value within the counting interval, in order to keep the module working. To reset the module you may also use any module specific instruction.
	The watchdog function is used as to monitor the connection between <i>ADwin</i> system and LS bus module.
	Valid for
	LS-2 Rev. A
	See also
	LS_DIO_Init, LS_DigProg, LS_Dig_IO, LS_Digout_Long, LS_Digin_ Long, LS_Get_Output_Status, LS_Watchdog_Init
	Example REM Example process for ADwin-Pro and 2 modules HSM-24V REM Set process to low priority! #INCLUDE ADwinPro_All.Inc
	<pre>INIT: PROCESSDELAY = 4000000 '10Hz HP REM Settings for LS module 2 via Pro module 3, channel 1 Par_1 = LS_DIO_INIT(3,1,2) Par_2 = LS_DIGPROG(3,1,2,01111b) 'channels 132 as output Par_3 = LS_WATCHDOG_INIT(3,1,2, 1, 1100) 'watchdog time 1.1 sections.</pre>
	<pre>REM Settings for LS module 4 via Pro module 3, channel 1 Par_11 = LS_DIO_INIT(3,1,4) Par_12 = LS_DIGPROG(3,1,4, 0h) 'channels 132 as input Par_13 = LS_WATCHDOG_INIT(3,1,4, 1, 1100) 'watchdog time 1.1 sec</pre>
	<pre>EVENT: REM set one channel to high, rotating from 1 to 32 INC Par_10 IF (Par_10 >= 32) THEN Par_10 = 0 Par_11 = SHIFT_LEFT(1,Par_10) REM set channels of LS module 2 LS_DIGOUT_LONG(3,1,2,Par_11) REM read channels of LS module 4 Par_15 = LS_DIGIN_LONG(3,1,4) REM reset watchdog LS_WATCHDOG_RESET(3,1)</pre>